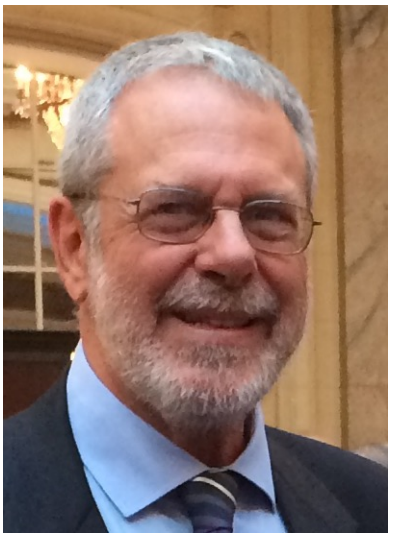
Manolis G.H. Katevenis



Detailed Curriculum Vitae

version 21 - last updated: July 2021

Manolis G.H. Katevenis,
Professor, Dept. of Computer Science, University of Crete; and
Head, Computer Architecture and VLSI Systems (CARV) Laboratory,
Institute of Computer Science (ICS),
Foundation for Research and Technology - Hellas (FORTH).
URL: http://users.ics.forth.gr/~kateveni
Telephone: +30-2811.39.1664 - Email: kateveni "at" ics.forth.gr
Mail/Courier/Visiting Address:
FORTH-ICS, 100 Plastira Avenue (Room AA282), Vassilika Vouton, Heraklion, Crete, GR-70013 GREECE.

Areas of Interest:
– *Computer Architecture:* Scalable, Low-Power, Manycore / Multiprocessor / Warehouse-Scale System Architecture for High Performance Computing (HPC) and Big Data; Exascale Computing; RISC-V;
– *Interprocessor Communication:* Memory-to-memory communication and synchronization – remote-write, remote-DMA, remote-enqueue; Lean, low-latency Network Interfaces;
– *Interconnection Network Architecture;*
– *VLSI Systems*.

Detailed CV of Manolis Katevenis - Table of Contents:

1. Positions Held, Education, Awards, Biography

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1.1 Positions Held:

Academic:
- **1996 - present:** Professor, Computer Science Department (CSD), University of Crete (UoC), Heraklion, Crete, Greece
- Chairman, Computer Science Department, University of Crete, Heraklion, Crete, Greece (**1994-96** and **1998-2000**)
- Associate Professor, Computer Science Department, University of Crete, Heraklion, Crete, Greece (**1992 - 1995**)
- Assistant Professor, Computer Science Department, University of Crete, Heraklion, Crete, Greece (**1986 - 1991**)
- Assistant Professor, Dept. of Computer Science, Stanford University, Stanford, California, USA (**1984 - 1985**)

Research:
- **1986 - present:** founder and Head, Computer Architecture and VLSI Systems (CARV) Laboratory, Institute of Computer Science (ICS), Foundation for Research and Technology - Hellas (FORTH), Heraklion, Crete, Greece. In the 80's, FORTH was called "Reseaerch Center of Crete", and CARV was called "Hardware Lab"; in the early 90's, CARV was called "Architecture and VLSI Group"; in 2005, CARV had grown considerably, and spun-off a part of it, which formed the Distributed Computing Systems (DCS) Laboratory; in 2021, CARV has a size of 80 to 100 members.
- **2004 - 2020:** European Network of Excellence on High-Perfomance and Embedded Architecture and Compilation (HiPEAC): founding partner and member of the Steering Committee.
- **2011 - 2020:** Co-founder, European Research Center on Computer Architecture, which became (2015-2020): EuroLab-4-HPC

Management:
- **2004 - 2021:** Deputy Director, Institute of Computer Science, FORTH.
- National Representative of Greece, ARTEMIS mirror group, European Commission (**2006** and **2007**)
- National Representative of Greece, ESPRIT Management Committee (ITC), European Commission (**1994 - 1998**)

Visiting:
- Visiting Faculty, Computer Science Division - EECS, University of California, Berkeley, CA USA (**1997** Fall Semester)
- Sabbatical at the Advanced Computer Research Institute (ACRI) S.A., Lyon, France (**1991** Fall Semester)
- Visiting Faculty, Department of Computer Science, Stanford University, Stanford, California, USA (**1987** Fall Semester)

1.2 Education:

- PhD. in Computer Science, University of California, Berkeley, CA USA (**1983**). Thesis: *Reduced Instruction Set Computer Architectures for VLSI*; Advisors: David Patterson and Carlo Sequin.
- MSc. in Electrical Engineering and Computer Science, University of California, Berkeley, CA USA (**1980**).
- Diploma of Electrical Engineering (GPA: 9.67), National Technical University of Athens (NTUA), Greece (**1978**).

1.3 Honors - Awards:

- Stelios Pichoridis Award for Outstanding Univesity Teaching – jointly with Charalampos Katerinopoulos – University of Crete, **2015**.
- Member of Academia Europaea - The Academy of Europe (Elected in **2012**).
- Award by the Secretary General of the Region of Crete **2003** – jointly with Stelios Orphanoudakis and Panos Constantopoulos – as the Principal Organizers of the Department of Computer Science, University of Crete.
- ACM Doctoral Dissertation Award **1984** "For his dissertation "Reduced Instruction Set Computer Architectures for VLSI." In 2015, the RISC Project was recognized as an **IEEE Milestone**.
- David J. Sakrison Memorial Prize **1983** - jointly with Robert Sherburne, Jr. - University of California, Berkeley.
- IBM PhD Fellowship, **1981 - 1983**, while a graduate student at the University of California, Berkeley.
- Greek State Fellowship for ranking first in his class, **1973 - 1978**, as undergraduate student at NTUA.

1.4 Biography:

Manolis G.H. Katevenis was born in Athens, Greece, in 1955; his parents were from Samos Island, in the Eastern Aegean Sea. He received his undergraduate degree in Mechanical and Electrical Engineering in 1978 from NTUA, Athens, Greece, and his M.Sc. (1980) and Ph.D. (1983) degrees in Computer Science from the University of California, Berkeley, USA. From January 1984 to March 1985 he was Assistant Professor of Computer Science at Stanford University, Stanford, California, USA. Since September 1985, he is with the *University of Crete*, Dept. of Computer Science, where he is currently a Professor; according to an Award by the Secretary General of the Region of Crete in 2003, Katevenis is recognized as one of the three Principal Organizers of this Department. Since 1985, he is also with the *Institute of Computer Science (ICS), FORTH*, Heraklion, Crete, where he founded and is since then the Head of the *Computer Architecture and VLSI Systems (CARV) Laboratory*. In 2012, he was elected Member of Academia Europaea - The Academy of Europe.

Katevenis was, in 2003-2004, a founding partner of HiPEAC, the European Network of Excellence on High-Performance and Embedded Architecture and Compilation, and was a member of its Steering Committee from 2004 till 2020. In 2011, he was one of the three founders of EuReCCA, the European Research Center on Computer Architecture, which gave birth, in 2015, to EuroLab-4-HPC. Katevenis is considered among the leading European Computer Architects, and recognized as the "father" of this field in his country, Greece. His key contributions in RISC architectures, interconnection networks, and interprocessor communication have appeared in more than 100 publications, and have received more than 3600 citations, with an h-index of 31. He has been principal investigator for over 30 RDI projects, with a total budget of over 18 Million Euro. Katevenis has been on the Technical Program Committees (PC's) or in other leading roles for more than 40 international conferences, he has given more than 60 conference talks and invited lectures, he has taught 16 different courses (8 of them graduate), having developed at least 5 of them, and he has supervised 50 graduate theses (14 of them: co-supervised), with some of the currently most prominent Greek computer architects (including two recipients of the ACM Maurice Wilkes award) being alumni of his.

His interests are in: Computer Architecture – Scalable, Low-Power, Manycore / Multiprocessor / Warehouse-Scale System Architecture for High Performance Computing (HPC) and Big Data, Exascale Computing, RISC-V; Interprocessor Communication and Synchronization, especially remote-write, remote-DMA, remote-enqueue based, and lean, low-latency Network Interfaces; Interconnection Network Architecture; and VLSI Systems.

During his doctoral studies (1980-83) under Carlo Sequin and David Patterson, Katevenis designed the micro-architecture of the RISC-I and RISC-II chips, and was the chief implementor of the *RISC-II* single-chip microprocessor at U.C.Berkeley (precursor of the SUN SPARC architecture), and for this thesis he received the 1983 Sakrison Memorial Prize and the 1984 ACM Doctoral Dissertation Award. The RISC ideas were adopted by the entire microprocessor industry and revolutionized this sector of technology in the late 80's. In 2015, the RISC Project was recognized as an *IEEE Milestone*, and in 2017 David Patterson, together with John Hennessy, received the ACM Turing Award for having led the RISC developments. The recently highly popular RISC-V free and open standard Instruction Set Architecture (ISA) is an evolution of that project; one part of the European Processor Initiative project, where CARV participates, is based on this ISA. After Berkeley, Katevenis consulted for AMD during the design of the "AMD-29000" RISC microprocessor, for Daisy Systems during the design of a hardware accelerator, for two other companies during the design of very-high speed RISC processors in ECL and GaAs, for a Storage Area Networking (SAN) company, and for DEC, SRC, where he did the preliminary switch design for "Autonet", precursor of DEC's "ATM GigaSwitch". In 1987, during the first meetings of the IEEE Standard 1596-1992 Scalable Coherent Interface (SCI) Committee, he was the first to propose using point-to-point connections rather than a bus architecture.

Katevenis made key world-wide contributions since 1986 in interconnection networks, which are central to implementing such diverse technologies as internet routers, multicore systems-on-chip, datacenter clusters, and supercomputers. Between 1986 and 1991, he made pioneering contributions in per-flow queueing, backpressure, congestion tolerance, and weighted round-robin scheduling, yielding weighted max-min fairness in switches for high speed networks –topics whose industrial application

was seen one or two decades later. In 1991 and 1992, he worked on switch design for multiprocessor interconnection networks. Between 1996 and 1998, Katevenis was the technical leader of the design of *ATLAS I*, a 6-million-transistor single-chip 16x16 ATM switch, implemented in 0.35-micron CMOS by ST Microelectronics, featuring 10 Gb/s throughput, sub-microsecond cut-through latency, and credit-based flow control (backpressure) at the granularity of 32 thousand virtual channels. In 1998-2001, he introduced *wormhole IP over ATM*, and led the design of pipelined heap management for schedulers in multi-gigabit weighted fair queueing, and hardware for managing thousands of queues in DRAM at 10 Gb/s line rate. In 2002-2005, his research concerned distributed scheduling in buffered crossbars, and non-blocking switching fabrics with internal backpressure. From 2006 to 2011, he worked on networks-on-chip (NoC), including the micro-architecture of high-radix on-chip crossbar switches. Since 2014, he works on dynamic max-min fair rate regulation for congestion management.

In parallel computing, Katevenis was among the pioneers in developing low-latency explicit interprocessor communication techniques. Katevenis' work in this area started in 1993-95, when he led the *Telegraphos* project in FORTH-ICS, where workstation clustering prototypes were designed and built, based on remote-write, remote-DMA, and remote-enqueue operations, including processor-network interfaces for protected user-level communication. Since 2006, his research concerns interprocessor communication, memory, and protection architecture in chip multiprocessors and in multi-chip, multi-blade, and multi-rack scalable systems. In the *SARC* project, he led the design of an architecture and FPGA prototype that unifies explicit and implicit communication by integrating the network interface with the cache controller, basing their common operation on a configurable event-response harware mechanism. In the *ENCORE* project, his group built prototypes of cache-optimized remote DMA and bare-metal runtime for systems with hundreds of cores but no cache coherence.

Since 2013, in the *EuroServer, ExaNeSt, ExaNoDe, EcoScale, EuroEXA*, and *RED-SEA* projects (where ExaNeSt was coordinated by Katevenis), his group builds prototypes of scalable, compact, and low-power processor and accelerator modules for *High Performance Computing (HPC)* and *Big Data* sytems. They are based on 64-bit ARM and RISC-V processors and they use a *Global Virtual Address Space* to enable low-latency remote-store, remote-DMA, and remote-enqueue based zero-copy, protected, user-level communication and synchronization; also, we investigated remote page borrowing, remote interrupts, and shared virtualized storage and I/O. The *ExaNeSt* prototype that was built in the CARV Lab has 768 processor cores in 192 FPGAs, with a total of 3 TBytes of DRAM and 12 TBytes of distributed SSD's, a rich custom interconnection network, and our own network interfaces. A full Linux software stack is running on it, including our own MPI library optimized for user-level RDMA, and the partners of the projects run entire real HPC Applications on the system.

For more information, see: http://users.ics.forth.gr/~kateveni

1.5 Selected Publications:

RISC Architectures:
- B1 (Ph.D. dissertation; ~360 citations)
- BC3 (in retrospect: the essence of the RISC idea)

Interconnection Network Architecture:
- J4 (JSAC'87: per-flow queueing, backpressure, round-robin scheduling, max-min fairness; ~160 citations)
- J5 (JSAC'91: weighted-round-robin scheduling; ~760 citations)
- J18 (Computer Networks '10: weighted max-min fairness)
- C11 (SIGCOMM'95: pipelined memory shared buffer; ~95 citations)
- C23 (HPCA'98: ATLAS I flow control; ~38 citations)
- C34 (Infocom'06: scheduling in buffered three-stage fabrics; ~50 citations)
- J15 (ToN'07: pipelined heap (priority queue) management; ~85 citations, including previous ICC'01 paper)
- J22 (TCAD'12: high-radix crossbars in VLSI)
- C53 (ANCS'15: energy consumption in Networks-on-Chip)
- C58 (NOCS'18: congestion management based on PA4)

Interprocessor Communication for Scalable Parallelism:
- C12 (HPCA'96: Telegraphos - remote-write/RDMA based, low-latency explicit interprocessor communication; ~70 citations, including previous Technical Report)
- C16 (HPCA'97: user-level, protected explicit interprocessor communication; ~40 citations)
- J17 (Micro'10: explicit interprocessor communication and synchronization in multi-core chips)
- C50 (ICS'13: software-guided prefetching using Task lifetimes and epoch-based cache replacement)
- J24 (JSA'14: the Formic 64-FPGA Prototype, emulating a 520-core heterogeneous manycore)
- J27 (Micpro'18: the ExaNeSt project, led by M. Katevenis, and its Prototype, built at FORTH-ICS CARV Laboratory)

2. Publications

last updated: July 2021

Citations:

Google Scholar Profile: scholar.google.com/citations?user=E2-GshsAAAAJ (on 10 Aug. 2021, shows 3649 citations, h-index = 31, i10-index = 63).

2.1 Books, Edited Books, Translated Books:

B4

M. Katevenis, M. Martonosi, C. Kozyrakis, O. Temam, T. Ungerer (Eds.): *Proceedings of the 6th International Conference on High Performance and Embedded Architectures and Compilers* - **HiPEAC 2011**, ACM Digital Library, ISBN: 978-1-4503-0241-8, Heraklion, Crete, Greece, 24-26 January 2011, 223 pages.

B3

P. Stenstrom, M. Dubois, M. Katevenis, R. Gupta, T. Ungerer (Eds.): *Proceedings, Third International Conference on High Performance Embedded Architectures and Compilers* - **HiPEAC 2008**, Goteborg, Sweden, Jan. 2008, 400 pages; LNCS 4917, Springer, ISSN 0302-9743, ISBN 978-3-540-77559-1.

B2

M. Mano: "*Digital Design*", Prentice-Hall, 1984, ISBN 0-13-212333-9. **Greek translation** by M. Katevenis with the assistance of a group of graduate students, Technical Chamber of Greece Editions, **1986**, 592 pages.

B1

M. Katevenis: "*Reduced Instruction Set Computer Architectures for VLSI*", 1984 ACM Doctoral Dissertation Award, MIT Press, ISBN 0-262-11103-9, **1985**. Full text of the Dissertation available on-line

2.2 Book Chapters (full-text reviewed):

BC4

S. Kavadias, M. Katevenis, D. Pnevmatikatos: "Network Interface Design for Explicit Communication in Chip Multiprocessors", Chapter 10 in the book: *Designing Network-on-Chip Architectures in the Nanoscale Era*, J. Flich and D. Bertozzi (Eds.), CRC Press - Taylor & Francis Groupa, ISBN: 978-1-4398-3710-8, **2011**, pp. 325-351.

BC3

M. Katevenis: "RISC Architectures", Chapter 20 in the book: *Parallel and Distributed Computing Handbook,* A. Zomaya Ed., McGraw-Hill, ISBN 0-07-073020-2, **1995**, pp. 595-620.

BC2

M. Katevenis: "The Nature of General-Purpose Computations", Chapter 2 (pp. 13-34) in the book: *Reduced Instruction Set Computers,* W. Stallings, Editor, IEEE Computer Society Press

Tutorial, 2nd Edition, ISBN 0-8186-8943-9, **1990**, pp. 13-34.

BC1

M. Katevenis, C. Sequin, D. Patterson, R. Sherburne: "RISC: Effective Architectures for VLSI Computers", Chapter 2 in the book: *VLSI Electronics: Microstructure Science - Vol. 14: VLSI Design,* N. Einspruch, Editor, Academic Press, ISBN 0-12-234114-7, **1986**, pp. 35-79.

2.3 Patents, Patent Applications:

PA4

M. Katevenis: "Dynamic Max-Min Fair Rate Regulation Apparatuses, Methods, and Systems", USA Patent US10158574B2, issued 18 Dec. 2018, and European Patent No. 3198810, issued 18 Feb. 2019 (Germany, France, UK). Foundation for Research and Technology -- Hellas (FORTH). Priority date: 24 Sep. 2014. patents.google.com/patent/US10158574B2 (full image PDF)

PA3

M. Katevenis, E. Markatos, P. Vatsolaki: "Notification of Message Arrival in a Parallel Computer System", Foundation for Research and Technology -- Hellas (FORTH), Heraklion Crete Greece, *European Patent Application No. 97410036.4-2201,* 19 March **1997**, Publication No. EP 0866406 A1 – the Remote Enqueue operation.

PA2

M. Katevenis: "A High-Throughput Data Buffer", Foundation for Research and Technology -- Hellas (FORTH), Heraklion Crete Greece, *USA Patent Number 5,774,653*, 2 August **1994**, issued 30 June 1998 – Pipelined Memory Shared Buffer for Switching.

PA1

M. Katevenis: "Method for processor simulation", ACRI S.A., Lyon, France, *European Patent Application EP19920420162*, 18 May **1992**, Publication No. EP 0570646 A1 – on-the-flight binary translation from a foreign to the local instruction set.

2.4 Journal Publications - full-text reviewed:

J27

M. Katevenis, et al.: "Next generation of Exascale-class systems: ExaNeSt project and the status of its interconnect and storage development", *Microprocessors and Microsystems: Embedded Hardware Design* **(MICPRO)**, Elsevier, vol. 61, Sep. 2018, pp. 58-71; DOI: 10.1016/j.micpro.2018.05.009

J26

N. Chrysos, L. Chen, C. Kachris, M. Katevenis: "Discharging the Network from its Flow Control Headaches: Packet Drops and HOL Blocking", *IEEE/ACM Transactions on Networking* **(ToN)**, vol. 24, no. 1, February 2016, pp. 15-28; DOI: 10.1109/TNET.2014.2378012

J25

G. Passas, M. Katevenis, D. Pnevmatikatos: "The Combined Input-Output Queued Crossbar Architecture for High-Radix On-Chip Switches", **IEEE Micro**, vol. 35, no. 6, November-December **2015**, pp. 38-47 (earlier published on-line: vol. PP, no. 99, June 2014); DOI: 10.1109/MM.2014.56

J24

S. Lyberis, G. Kalokerinos, M. Lygerakis, V. Papaefstathiou, I. Mavroidis, M. Katevenis, D. Pnevmatikatos, D.S. Nikolopoulos: "FPGA prototyping of emerging manycore architectures for parallel programming research using Formic boards", *Journal of Systems Architecture* **(JSA)**, Elsevier, vol. 60, issue 6, June **2014**, pp. 481-493; DOI: 10.1016/j.sysarc.2014.03.002

J23

C. Kachris, G. Nikiforos, V. Papaefstathiou, S. Kavadias, M. Katevenis: "NP-SARC: Scalable network processing in the SARC multi-core FPGA platform", *Journal of Systems Architecture* **(JSA)**, Elsevier, vol. 59, issue 1, January **2013**, Pages 39-47; DOI: 10.1016/j.sysarc.2012.11.001

J22

Giorgos Passas, Manolis Katevenis, Dionisios Pnevmatikatos: "Crossbar NoCs Are Scalable Beyond 100 Nodes", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* **(TCAD)**, ISSN: 0278-0070, vol. 31, issue 4, April **2012**, pp. 573-585; DOI: 10.1109/TCAD.2011.2176730

J21

Dario Suarez Gracia, G. Dimitrakopoulos, T. Monreal Arnal, M. Katevenis, V. Vinals Yufera: "LP-NUCA: Networks-in-Cache for High-Performance Low-Power Embedded Processors", *IEEE Transactions on Very Large Scale Integrated Systems* **(TVLSI)**, vol. 20, no. 8, August **2012**, pp. 1510-1523 (earlier published on-line: vol. PP, no. 99, July 2011); DOI: 10.1109/TVLSI.2011.2158249

J20

S. Kavadias, M. Katevenis, M. Zampetakis, D. Nikolopoulos: "Cache-Integrated Network Interfaces: Flexible On-Chip Communication and Synchronization for Large-Scale CMPs", *Int. Journal of Parallel Programming* **(IJPP)**, Springer, vol. 40, issue 6, December **2012**, pp. 583-604; (earlier published on-line: June 2011); DOI: 10.1007/s10766-011-0173-6

J19

G. Kalokerinos, V. Papaefstathiou, G. Nikiforos, S. Kavadias, M. Katevenis, D. Pnevmatikatos, X. Yang: "Prototyping a Configurable Cache/Scratchpad Memory with Virtualized User-Level RDMA Capability", *Transactions on HiPEAC* **(ToH)**, vol. 5, no. 3, **2010**.

J18

N. Chrysos, M. Katevenis: "Distributed WFQ scheduling converging to weighted max-min fairness", **Computer Networks** (Elsevier), ISSN 13891286, vol. 55, issue 3, Oct. **2010** (on-line), Feb. 2011 (in print), pp. 792-806.

J17

M. Katevenis, V. Papaefstathiou, S. Kavadias, D. Pnevmatikatos, F. Silla, D. Nikolopoulos: "Explicit Communication and Synchronization in SARC", **IEEE Micro**, vol. 30, no. 5, pp. 30-41, Sep./Oct. **2010**.

J16

D. Simos, I. Papaefstathiou, M. Katevenis: "Building an FoC Using Large, Buffered Crossbar Cores", **IEEE Design & Test**, vol. 25, no. 6, pp. 538-548, Nov. **2008**; DOI: 10.1109/MDT.2008.159

J15

A. Ioannou, M. Katevenis: "Pipelined Heap (Priority Queue) Management for Advanced Scheduling in High Speed Networks", *IEEE/ACM Transactions on Networking* **(ToN)**, vol. 15, no. 2, pp. 450-461, April **2007**; DOI: 10.1109/TNET.2007.892882

J14

G. Sapountzis, M. Katevenis: "Benes Switching Fabrics with O(N)-Complexity Internal Backpressure", **IEEE Communications Magazine** vol. 43, no. 1, pp. 88-94, January **2005**.

J13

E. Markatos, D. Pnevmatikatos, M. Flouris, M. Katevenis: "Web-Conscious Storage Management for Web Proxies", *IEEE/ACM Transactions on Networking* **(ToN)**, vol. 10, no. 6, pp. 735-748, Dec. **2002**; DOI: 10.1109/TNET.2002.804836

J12

M. Katevenis, Iakovos Mavroidis, G. Sapountzis, E. Kalyvianaki, Ioannis Mavroidis, G. Glykopoulos: "Wormhole IP over (Connectionless) ATM", *IEEE/ACM Transactions on Networking* **(ToN)**, vol. 9, no. 5, pp. 650-661, October **2001**; DOI: 10.1109/90.958332

J11

M. Katevenis, E. Markatos, P. Vatsolaki, C. Xanthaki: "The Remote Enqueue Operation on Networks of Workstations", *Informatica - an International Journal of Computing and Informatics*, ISSN 0350-5596, 23(1), pp. 29-39, April **1999**.

J10

G. Kornaros, D. Pnevmatikatos, P. Vatsolaki, G. Kalokerinos, C. Xanthaki, D. Mavroidis, D. Serpanos, M. Katevenis: "ATLAS I: Implementing a Single-Chip ATM Switch with Backpressure", **IEEE Micro**, vol. 19, no. 1, pp. 30-41, Jan/Feb. **1999**.

J9

D. Serpanos, M. Katevenis, E. Spyridakis: "ATLAS I: Building Block for ATM Networks with

Credit-based Flow Control", *IEICE Trans. on Communications,* Japan, **1998**.

J8

M. Katevenis, D. Serpanos, G. Dimitriadis: "ATLAS I: A Single-Chip, Gigabit ATM Switch with HIC/HS Links and Multi-Lane Back-Pressure", *Microprocessors and Microsystems,* Elsevier, vol. 21, no. 7-8, pp. 481-490, March **1998**; DOI: 10.1016/S0141-9331(98)00041-6

J7

M. Katevenis, E. Markatos, G. Kalokerinos, A. Dollas: "Telegraphos: A Substrate for High Performance Computing on Workstation Clusters", *Journal of Parallel and Distributed Computing* **(JPDC)**, Academic Press, vol. 43, no. 2, pp. 94-108, June **1997**; DOI: 10.1006/jpdc.1997.1334

J6

M. Katevenis, P. Vatsolaki, V. Chalkiadakis: "Credit-Flow-Controlled ATM over HIC Links in the ASICCOM "ATLAS I" Single-Chip Switch", *Real-Time Magazine,* vol. 96, no. 3, pp. 65-72, July **1996**.

J5

M. Katevenis, S. Sidiropoulos, C. Courcoubetis: "Weighted Round-Robin Cell Multiplexing in a General-Purpose ATM Switch Chip", *IEEE Journal on Selected Areas in Communications* **(JSAC)**, Vol. 9, No. 8, pp. 1265-1279, October **1991**; DOI: 10.1109/49.105173

J4

M. Katevenis: "Fast Switching and Fair Control of Congested Flow in Broad-Band Networks", *IEEE Journal on Selected Areas in Communications* **(JSAC)**, Vol. 5, No. 8, pp. 1315-1326, October **1987**.

J3

R. Sherburne, M. Katevenis, D. Patterson, C. Sequin: "A 32-Bit NMOS Microprocessor with a Large Register File", *IEEE Journal of Solid State Circuits* **(JSSC)**, Vol. 19, No. 5, pp. 682-689, October **1984**; DOI: 10.1109/JSSC.1984.1052208

J2

M. Katevenis, R. Sherburne, D. Patterson and C. Sequin: "The RISC II Micro-Architecture", *Journal of VLSI and Computer Systems,* Computer Science Press Inc., vol. 1, issue 2, September **1984**, pp. 138-152.

J1

D. Fitzpatrick, J. Foderaro, M. Katevenis, H. Landman, D. Patterson, J. Peek, Z. Peshkess, C. Sequin, R. Sherburne, K. VanDyke: "A RISCy Approach to VLSI", *VLSI Design Magazine,* Vol. II, No. 4, 4th qu. **1981**, pp. 14-20.

2.5 Conference and Major Workshop Proceedings Publications - full-text reviewed:

C62

A. Psistakis, N. Chrysos, F. Chaix, M. Asiminakis, M. Giannioudis, P. Xirouchakis, V. Papaefstathiou, M. Katevenis: "PART: Pinning Avoidance in RDMA Technologies", Proc. of the *14th IEEE/ACM Int. Symp. on Networks-on-Chip* (**NOCS 2020**), Hamburg, Germany, 24-25 Sep. 2020, pp. 1-8; DOI: 10.1109/NOCS50636.2020.9241587

C61

G. Taffoni, L. Tornatore, D. Goz, A. Ragagnin, S. Bertocco, I. Coretti, M. Marazakis, F. Chaix, M. Plumidis, M. Katevenis, R. Panchieri, G. Perna: "Towards Exascale: Measuring the Energy Footprint of Astrophysics HPC Simulations", Proc. of the *15th IEEE Int. Conf. on e-Science and Grid Computing* (**eScience 2019**), San Diego, CA, USA, 24-27 Sep. 2019, pp. 403-412; DOI: 10.1109/eScience.2019.00052

C60

M. Ploumidis, N. Kallimanis, M. Asiminakis, N. Chrysos, P. Xirouchakis, M. Gianoudis, L. Tzanakis, N. Dimou, A. Psistakis, P. Peristerakis, G. Kalokairinos, V. Papaefstathiou, M. Katevenis: "Software and Hardware Co-design for Low-Power HPC Platforms", *ISC High Performance 2019 Int. Workshops Revised Selected Papers*, Frankfurt, Germany, 16-20 June 2019, **LNCS 11887**, Springer, Cham, pp. 88-100; DOI: 10.1007/978-3-030-34356-9_9

C59

G. Pitsis, G. Tsagkatakis, C. Kozanitis, I. Kalomoiris, A. Ioannou, A. Dollas, M. Katevenis, P. Tsakalides: "Efficient Convolutional Neural Network Weight Compression for Space Data Classification on Multi-FPGA Platforms", Proc. of the *2019 IEEE Int. Conf. on Acoustics, Speech and Signal Processing* (**ICASSP 2019**), Brighton, UK, 12-17 May 2019, pp. 3917-3921; DOI: 10.1109/ICASSP.2019.8682732

C58

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C57

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(The IEEE "Superbus" Study Group was formed in 1987 in order to standardize a backplane bus in the 1 GByte/s throughput range. This was the first proposal to the group to base the new standard on a ring of point-to-point connections rather than a bus. The Study Group later adopted this idea, renamed the project "Scalable Coherent Interface" (SCI), and developed ANSI/IEEE Standard 1596 (1992), which is based on rings of point-to-point connections).

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[RISC 1980] M. Katevenis: "A Proposal for the LSI Implementation of the RISC I CPU (using a 3-phase clock)", *U.C.Berkeley, CS Div., Internal Working Paper,* September 1980.
(This internal working paper has served as the specification (block structure and timing) for the VLSI design of the RISC I NMOS single-chip 32-bit processor).

3. Research Grants, Commercialization Efforts

last updated: July 2021

3.0 Recent EuroHPC Projects attracted to the CARV Laboratory:

Recent (2021 onwards) Research and Innovation projects, co-funded by the EuroHPC JU and the Greek Government, that have been attracted to the CARV Laboratory of FORTH-ICS mostly as a result of the successful track record of CARV in the preceding projects, especially EPI-SGA1 and ExaNeSt-ExaNoDe-EcoScale-EuroEXA, as well as SARC-ENCORE-EuroServer before them; Manolis Katevenis played an important role as Principal Investigator (PI) or co-PI in these preceding projects, but no longer serves as project PI after 2021:

→ Press Releases (in Greek): Greece ranked 5th among European countries in EuroHPC-2019; Crete participation in EuroHPC-2019; and a TV interview on these topics.

- European Processor Initiative (EPI) FPA – SGA2 (2021-2024, Call: EuroHPC-2020-02) – *currently under negotiation*. **PI: Vassilis Papaefstathiou; Co-PI: Manolis Marazakis**. Coordinating partner: BULL/ATOS, France. Continuation of EPI SGA1.

- **EUPEX** "European Pilot for Exascale" (2022-2025, Call: EuroHPC-2020-01-a "Advanced pilots towards the European supercomputers" - Pilot-1 of 2) – *currently under negotiation*. **PI: Angelos Bilas**. Coordinating partner: BULL/ATOS, France.

- **The European PILOT** "Pilot using Independent Local & Open Technologies" (2021-2025, Call: EuroHPC-2020-01-a "Advanced pilots towards the European supercomputers" - Pilot-2 of 2) – *currently under negotiation*. **PI: Vassilis Papaefstathiou; Co-PI: Manolis Marazakis**. Coordinating partner: BSC, Spain.

- eProcessor: "European, extendable, energy-efficient, energetic, embedded, extensible, Processor Ecosystem" (*1/4/2021 - 31/03/2024*; EuroHPC 956702; Call: EuroHPC-01-2019 "Extreme scale computing and data driven technologies" - project (a) among four large projects called). **PI: Vassilis Papaefstathiou**. FORTH-ICS budget: **1367 k€**. Coordinating partner: BSC, Spain. FORTH-ICS leads the Work-Package on System Simulation and FPGA Emulation, and additionally contributes the L2 Cache.

- RED-SEA: "Network Solution for Exascale Architectures" (*1/4/2021 - 31/03/2024*; EuroHPC 955776; Call: EuroHPC-01-2019 "Extreme scale computing and data driven technologies" - project (c) among four large projects called). **PI: Nikolaos Chrysos**. FORTH-ICS budget: **932 k€**. Coordinating partner: BULL/ATOS, France. FORTH-ICS leads the Work-Package on Endpoint Functions and Reliability, and contributes especially in congestion management and in lean, tightly-coupled RISC-V network interfaces.

- DEEP-SEA: "DEEP - Software for Exascale Architectures" (*1/4/2021 - 31/03/2024*; EuroHPC 955606; Call: EuroHPC-01-2019 "Extreme scale computing and data driven technologies" - project (d) among four large projects called). **PI: Manolis Marazakis**. FORTH-ICS budget: **1292 k€**. Coordinating partner: Julich, Germany.

3.1 R&D Grants by the European Commission:

Research, Development, and Innovation projects at FORTH-ICS, funded by the European Commission following an evaluation of competing proposals, where Manolis Katevenis was the *Principal Investigator (PI)* at FORTH-ICS, or *co-PI* where noted as such:

- European Processor Initiative (EPI) FPA – SGA1 (*1/12/2018 - 30/11/2021*; H2020 ICT 826647), **co-PI with Vassilis Papaefstathiou and Manolis Marazakis**. FORTH-ICS budget: **2914 k€**. Coordinating partner: BULL/ATOS, France. FORTH-ICS contributes the L2 Cache of the RISC-V

based accelerator, and makes important contributions in co-design and simulation, in systems software, in the Software Development Vehicle, and in verification, testing, and bringup.

- EuroEXA: "Co-designed Innovation and System for Resilient Exascale Computing in Europe: from Applications to Silicon" (*1/9/2017 - 31/12/2021*; H2020 FET-HPC 754337), **co-PI with Polyvios Pratikakis and Manolis Marazakis**. FORTH-ICS budget: **1245 k€**. Coordinating partner: ICCS, Athens, Greece. FORTH-ICS leads the Work-Package on Systems Software and Programming Environment, and contributes also in firmware, interconnects, accelerators, applications, and in supporting the project's Prototypes.

- EcoScale: "Energy-efficient Heterogeneous COmputing at exaSCALE" (FORTH participation is during *1/1/2018 - 31/7/2019*; H2020 FET-HPC 671632). FORTH-ICS budget: **263 k€**. Coordinating partner: TSI, Chania, Crete, Greece. FORTH-ICS contributes in building the project's Prototype.

- ExaNeSt: "European Exascale System Interconnect and Storage" (*1/12/2015 - 31/5/2019*; H2020 FET-HPC 671553). FORTH-ICS is the **Coordinating** partner, and **Manolis Katevenis was the Coordinator** of the entire Consortium. FORTH-ICS budget: **2190 k€**. Overall project budget: **8440 k€**. FORTH-ICS contributes mainly in designing and building the Prototype, in the Interconnection Network Architecture, and in the Storage Systems Software.

- ExaNoDe: "European Exascale Processor Memory Node Design" (*1/10/2015 - 31/3/2019*; H2020 FET-HPC 671578). FORTH-ICS budget: **1092 k€**. Coordinating partner: CEA, France. FORTH-ICS contributes mainly in the Prototype design and in Systems Software.

- EuroLab4HPC2: "Foundations of a European Research Center of Excellence in High-Performance Computing Systems" (*1/5/2018 - 30/4/2020*; H2020 CSA 800962). FORTH-ICS budget: **56 k€**. Coordinating partner: Chalmers University of Technology, Sweden.

- EuroLab-4-HPC: "Foundations of a European Research Center of Excellence in High-Performance Computing Systems" (*1/9/2015 - 31/8/2017*; H2020 CSA 671610). FORTH-ICS budget: **80 k€**. Coordinating partner: Chalmers University of Technology, Sweden. FORTH-ICS leads the HPC Curriculum and the Dissemination and Engagement Events.

- HiPEAC-5: "High Performance and Embedded Architecture and Compilation" (*1/12/2017 - 29/2/2020*; H2020 CSA 779656). FORTH-ICS budget: **35 k€**. Coordinating partner: Ghent University, Belgium. FORTH-ICS: leading the Computing Systems Weeks task.

- HiPEAC-4: "High Performance and Embedded Architecture and Compilation" (*1/1/2016 - 28/2/2018*; H2020 CSA 687698). FORTH-ICS budget: **80 k€**. Coordinating partner: Ghent University, Belgium. FORTH-ICS: leading the Computing Systems Weeks task.

- EuroServer: "Green Computing Node for European Micro-Servers" (*1/9/2013 - 31/1/2017*; ICT FP7 IP 610456), **co-PI with Angelos Bilas**. FORTH-ICS budget: **1515 k€**. Coordinating partner: CEA, France. Katevenis responsible for: architectural design and FPGA prototyping for advanced features in the interconnection network and the memory system.

- HiPEAC-3: European Network of Excellence on "High Performance and Embedded Architecture and Compilation" (*1/2/2012 - 29/2/2016*; ICT FP7 NoE 287759). FORTH-ICS budget: **160 k€**. Coordinating partner: Ghent University, Belgium. FORTH-ICS task: leading the Computing Systems Weeks task; responsible for the Workgroups on Interconnection Networks and on Scalable Storage and I/O; co-responsible for the Workgroup on Parallel Programming Languages and Models.

- HiPEAC-2: European Network of Excellence on "High Performance and Embedded Architecture and Compilation" (*1/2/2008 - 31/1/2012*; ICT FP7 NoE 217068). FORTH-ICS budget: **388 k€**. Coordinating partner: Ghent University, Belgium. FORTH-ICS task: Coordinator of the Interconnects Research Cluster and of the Task Force on Education and Training.

- ENCORE: "ENabling technologies for a programmable many-CORE" (*1/3/2010 - 28/2/2013*; ICT FP7 STREP 248647), **co-PI with Dimitris Nikolopoulos**. FORTH-ICS budget: **533 k€**. Coordinating partner: Barcelona Supercomputing Center. Katevenis responsible for: architectural support and FPGA prototype for explicit communication in parallel processing on many-cores.

- SARC: "Scalable Computer Architecture" (*1/1/2006 - 31/3/2010*; FP6 FET IP 027648). FORTH-ICS budget: **1200 k€**. Coordinating partner: T.U. Delft, Netherlands. Katevenis responsible for: architectural support and FPGA prototype for low-latency, explicit interprocessor communication.

- HiPEAC-1: European Network of Excellence on "High Performance Embedded Architecture and Compilation" (*1/9/2004 - 31/12/2008*; ICT FP6 NoE 004408), **co-PI with Angelos Bilas**. FORTH-ICS budget: **246 k€**. Coordinating partner: UPC, Barcelona, Spain. FORTH-ICS task: research in computer architecture and in particular in interconnection networks, common computing equipment.

- SIVSS: "Scaleable Intelligent Video Server System" (*1/1/2004 - 31/10/2006*; ICT FP6 STREP), **co-PI with Angelos Bilas**. FORTH-ICS budget: **820 k€**. Coordinating partner: Xyratex Ltd, UK. Katevenis responsible for: novel architectural features for building scalable switches, switching fabrics, and low-latency network interfaces.

- **SPEAR-2**: 8-month feasibility study on a cost effective version of the SPARClet architecture dedicated to broadcast media embedded application (*1/12/1997 - 31/7/1998*). FORTH-ICS budget: **160 k€**. Coordinating partner: TSQWARE, France.

- **ARCHES**: "Application, Refinement, and Consolidation of HIC, Exploiting Standards" (*1995 - 1997*; ESPRIT IV). FORTH-ICS budget: **300 k€**. Coordinating partner: SGS Thomson, UK. FORTH-ICS task: participation in the architecture design of advanced network adapters.

- **ASICCOM**: "ATM Switch for Integrated Communication, Computation, and Monitoring" (*1/9/1995 - 31/5/1999*; ACTS 060). FORTH-ICS budget: **1400 k€**. Coordinating partner: Intracom S.A., Peania, Greece. Technical Coordinator for the entire Project: M. Katevenis. FORTH-ICS task: architecture and chip design of *ATLAS I*, a 6-million-transistor single-chip 16x16 ATM switch with 32 thousand virtual channels of credit-based flow control; the chip was fabricated by ST Microelectronics.

- **AMUS** and **SHIPS**: "A Multiscalar Supercomputer" and "Supercomputer Highly Parallel System" (*1/1/1991 - 31/5/1995*; ESPRIT II 2716, ESPRIT III 6253). FORTH-ICS budget: **1800 k€**. Coordinating partner: Advanced Computer Research Institute (ACRI) S.A., Lyon, France. FORTH-ICS task: architectural studies for a parallel supercomputer; and the *Telegraphos* project: architecture, design, and implementation of prototypes for remote-write and remote-DMA based high-speed communication in parallel and distributed systems.

- **Hellenic-VLSI**: "Hellenic VLSI Design & Prototyping Environment" (*1/1/1991 - 31/12/1993*; ESPRIT II 5692 and STRIDE). FORTH-ICS budget: **210 k€**. FORTH-ICS task: designing a JPEG image-compression chip, and a control unit for a VHF amplifier.

3.2 Commercialization Efforts:

Manolis Katevenis has worked extensively, either as *Principal Investigator (PI)* himself, or as *Head of the CARV Laboratory* of FORTH-ICS assisting the PI in this Laboratory, in the following major efforts to attract high-tech industry to Crete and to commercialize R&D results of the CARV Laboratory:

- Iakovos Mavroidis, a member of CARV, cofounded (*2020*) together with Ioannis Papaefstathiou, EXAPSYS, *Exascale Performance Systems Plc*., a start-up company in Greece, focusing on HPC systems and applications.
- KALEAO Ltd. (UK) set up (*2015-2018*) its first main Engineering/Development Lab in the Science and Technology Park of Crete (STEP-C), in the FORTH Campus in Heraklion, Crete. KALEAO was a spin-off company of the EuroServer project. Manolis Katevenis, with the assistance of Iakovos Mavroidis, Manolis Marazakis, and a team of 20, led the efforts to attract KALEAO to Crete.
- Angelos Bilas, a member of CARV, attracted (*2013-2019*) a North American company, ioFabric, in

the Storage domain to establish its Engineering Team in STEP-C, within the FORTH Campus.
- Angelos Bilas, a member of CARV, commercialized (*2012*) a subsystem in storage software, dealing with Solid-State-Disk (SSD) Caching, through NEVEX, a Canadian company, to a very large international company.
- Angelos Bilas made efforts in *2008* to commercialize storage software with a company called *Cronera*. Later (*2012-2016*), he has had analogous collaboration with the German part of a large international company.
- Christos Sotiriou, an ex-member of CARV, with the assistance of Manolis Katevenis, made extensive commercialization efforts (*2006 - 2009*) in the domain of Computer-Aided Design (CAD) tools for combating the problem of variability in VLSI, through a company called *Nanochronous Logic*.

- Manolis Katevenis worked (*1998 - 2000*) with Christos Skalkos of AMCC (large USA company in the communications chips area) with the goal of attracting AMCC to establish a chip design center in Greece.
- Manolis Katevenis worked (*1991 - 1994*) with Tor Bloch, CEO of ACRI (French start-up company in Supercomputers) with the goal of attracting ACRI to establish a design center in Crete.
- Manolis Katevenis worked (*1988 - 1989*) with George Perlegos, CEO of ATMEL (large USA company in the integrated circuits area) with the goal of attracting ATMEL to establish a chip design center in Crete.

3.3 R&D Grants from the Private Sector:

Research and development contracts to FORTH-ICS from private-sector companies, where Manolis Katevenis was/is the *Principal Investigator (PI)* at FORTH-ICS, or *co-PI* where noted as such:

- **Ellemedia** S.A., Athens, Greece (*2003 - 2006*), **co-PI with Ioannis Papaefstathiou**; FORTH-ICS budget: **160 k€**. FORTH-ICS task: Subsystem design and coding for ASIC and FPGA systems - MEDIAGATE, NPMADE, WEBSOC.
- **INACCESS** S.A., Athens, Greece (*2002 - 2003*), **co-PI with Ioannis Papaefstathiou**; FORTH-ICS budget: **45 k€**. FORTH-ICS task: DES and MMU subsystem design for ASIC's.
- **ISD** S.A., Athens, Greece (*2000 - 2003*); FORTH-ICS budget: **47 k€**. FORTH-ICS task: subsystem design for ASIC- and PCB-based digital systems.
- **Intracom** S.A., Athens, Greece (*1998 - 1999*); FORTH-ICS budget: **50 k€**. FORTH-ICS task: interfacing the ATLAS I switch chip (from the ASICCOM project) to a standard ATM network with OC-12 links (FASMA, MEMAS).

- **NISHAN** Systems Inc, San Jose, California USA (*1999 - 2001*); FORTH-ICS budget: **150 k€**. FORTH-ICS task: Consulting to Nishan Systems Inc. on Packet Switch Architectures and Chip Design for Storage Area Networks

3.4 R&D Grants by the Greek Government:

Research and development projects at FORTH-ICS funded by the Greek Government following an evaluation of competing proposals, where Manolis Katevenis was/is the *Principal Investigator (PI)* at FORTH-ICS, or *co-PI* where noted as such:

- **GreenVM**: "Energy-Efficient Runtimes for Scalable Multicore Architectures" (*2012 - 2015*; ARISTEIA-I), **co-PI with Panagiota Fatourou**. FORTH-ICS is the sole contractor, with budget: **486 k€**.
- **PLATON** (*2000 - 2001*; PENED): FORTH-ICS budget: **65 k€**.
- **DIPOLO**: packet router implementation, at the PCB and embedded processor level, with advanced QoS features (*1999 - 2001*; EPET II); FORTH-ICS budget: **175 k€**.
- **EPET-Microelectronics**: "Development of Industrial Microelectronics products" (*1/7/1995 - 31/12/1997*; EPET II 476). FORTH-ICS budget: **40 k€**.
- **MOP-CAD**: "Mediterranean Integrated Program on Computer Aided Design" (*1987 - 1992*). FORTH-ICS budget: **400 k€**. FORTH-ICS task: CAD tools for various engineering disciplines.

3.5 Host Scientist for New Researchers with Marie-Curie Grants:

Manolis Katevenis was the *Host Scientist* for new researchers that came to FORTH-ICS funded by the following Marie-Curie European Commission Mobility Grants:

- **I-Cores**: "I-cores - Hypervisor-Based Synthesis of Custom Execution Environments on Multi-Core Systems" (*1/12/2008 - 30/11/2012*, int. reintegration grant). Principal Investigator: *Dimitris Nikolopoulos*; FORTH-ICS budget: **100 k€**.
- **ATHLOS** (*2004-2008*), int. reintegration grant. Principal Investigator: *Angelos Bilas*; FORTH-ICS budget: **80 k€**.
- **UNiSIX**: "Unifying High-speed Interconnects" (*1/2/2005 - 31/1/2009*, Marie-Curie Excellent Team). Principal Investigator: *Angelos Bilas*; FORTH-ICS budget: **1163 k€**.

4. Editorial and Conference Organization, PC Memberships

last updated: July 2021

4.1 Editorial Board:

Manolis Katevenis was a member of the Editorial Board of the *Transactions on High-Performance and Embedded Architectures and Compilers (Transactions on HiPEAC)* - http://www.hipeac.net/journal

4.2 General Co-Chair:

Manolis Katevenis and Margaret Martonosi were General Co-Chairs for the *6th International Conference on High-Performance and Embedded Architectures and Compilers - HiPEAC'11*, Heraklion, Crete, Greece, 24-26 January 2011; http://www.hipeac.net/hipeac2011

4.3 Technical Program Committee (PC) Co-Chair:

- **ICS 2012**: Gianfranco Bilardi and Manolis Katevenis were Program Co-Chairs for the *26th ACM International Conference on Supercomputing - ICS 2012*, Venice, Italy, June 2012; http://ics-conference.org
- **HiPEAC 2008**: Manolis Katevenis and Rajiv Gupta were Program Co-Chairs for the *3rd International Conference on High Performance Embedded Architectures and Compilers - HiPEAC 2008*, Goteborg, Sweden, 27-29 January 2008; http://www.hipeac.net/hipeac2008

4.4 Technical Program Committee (PC) Member:

Manolis Katevenis was a Member of the Technical Program Committees for the following Conferences:

- **SAMOS 2017** (IEEE Int. Conf. on Embedded Computer Systems: Architectures, Modeling and Simulation): Samos, Greece, 17-20 July 2017; samos-conference.com/[2017]
- **SAMOS 2016** (IEEE Int. Conf. on Embedded Computer Systems: Architectures, Modeling and Simulation): Samos, Greece, 18-21 July 2016; samos-conference.com/[2016]
- **SAMOS 2015** (IEEE Int. Conf. on Embedded Computer Systems: Architectures, Modeling and Simulation): Samos, Greece, 20-23 July 2015; samos-conference.com/[2015]
- **HiPEAC 2015** (Int. Conf. on High-Performance and Embedded Architectures and Compilers), Amsterdam, Netherlands, 19-21 Jan. 2015 (as a member of the Board of Distinguished Reviewers for ACM Tr. on Architecture and Code Optimization (TACO) during the year 2014).
- **SAMOS 2014** (IEEE Int. Conf. on Embedded Computer Systems: Architectures, Modeling and Simulation): Samos, Greece, 14-17 July 2014; samos-conference.com/[2014]
- **HiPEAC 2014** (Int. Conf. on High-Performance and Embedded Architectures and Compilers),

Vienna, Austria, 20-22 Jan. 2014 (as a member of the Board of Distinguished Reviewers for ACM Tr. on Architecture and Code Optimization (TACO) during the year 2013).
- **SAMOS 2013** (IEEE Int. Conf. on Embedded Computer Systems: Architectures, Modeling and Simulation): Samos, Greece, 15-18 July 2013; samos-conference.com/[2013]
- (External Review Committee member, 45th Annual IEEE/ACM Int. Symp. on Microarchitecture - MICRO 2012, Vancouver, Canada, 1-5 Dec. 2012)
- **SAMOS 2012** (IEEE Int. Conf. on Embedded Computer Systems: Architectures, Modeling and Simulation): Samos, Greece, 16-19 July 2012; samos-conference.com/[2012]
- **HiPEAC 2012** (Int. Conf. on High-Performance and Embedded Architectures and Compilers), Paris, France, 23-25 Jan. 2012; http://www.hipeac.net/hipeac2012
- **HiPC 2011** (18th Annual IEEE Int. Conf. on High Performance Computing), Bengaluru (Bangalore), India, 18-21 Dec. 2011; http://www.hipc.org/hipc2011/
- **SAMOS 2011** (IEEE Int. Conf. on Embedded Computer Systems: Architectures, Modeling and Simulation): Samos, Greece, 18-21 July 2011; samos-conference.com/[2011]
- **Cluster 2010** (IEEE Int. Conf. on Cluster Computing 2010): Heraklion, Crete, Greece, 20-24 Sep. 2010; http://www.cluster2010.org
- **SAMOS 2010** (IEEE Int. Conf. on Embedded Computer Systems: Architectures, Modeling and Simulation): Samos, Greece, 20-23 July 2010; samos-conference.com/[2010]
- **NOCS 2010** (4th ACM/IEEE Int. Symp. on Networks-on-Chip): Grenoble, France, 3-6 May 2010; http://www.minatec.org/nocs2010/
- **ANCS 2009** (5th ACM/IEEE Symp. on Architectures for Networking and Communications Systems): Princeton, NJ, USA, 19-20 Oct. 2009; http://www.ancsconf.org
- **ICPP 2009** (8th Int. Conf. on Parallel Processing): Vienna, Austria, 22-25 Sep. 2009; http://www.cse.ohio-state.edu/~icpp2009/
- **SAMOS 2009** (International Workshop on Systems, Architectures, Modeling, and Simulation - SAMOS Workshop): Samos, Greece, 20-23 July 2009; samos-conference.com/[2009]
- **NOCS 2009** (3rd ACM/IEEE Int. Symp. on Networks-on-Chip): San Diego, CA, USA, 10-13 May 2009; http://circuit.ucsd.edu/~nocs2009/
- **ARCS'09** (22nd Int. Conf. on Architecture of Computing Systems): T.U.Delft, Netherlands, 10-13 Mar. 2009; http://www.ida.ing.tu-bs.de/arcs09/
- **ANCS 2008** (4th ACM/IEEE Symp. on Architectures for Networking and Communications Systems): San Jose, CA, USA, 6-7 Nov. 2008; http://www.ancsconf.org
- **dasCMP 2008** (Workshop on Design, Architecture and Simulation of Chip Multi-Processors, held in conjunction with the 41st Annual International Symposium on Microarchitecture): Lake Como Italy, 9 Nov. 2008; http://passat.crhc.uiuc.edu/dasCMP
- **HPSR 2008** (IEEE International Conference on High Performance Switching and Routing): Shanghai, China, 15-17 May 2008; http://www.hpsr2008.odu.edu/
- **SAMOS VIII** (International Workshop on Systems, Architectures, Modeling, and Simulation - SAMOS Workshop): Samos, Greece, 21-24 July 2008; samos-conference.com/[2008]
- **ANCS 2007** (3rd ACM/IEEE Symp. on Architectures for Networking and Communications Systems): Orlando, Florida, USA, 3-4 Dec. 2007; http://www.ancsconf.org
- **ICS'07** (21st ACM Int. Conf. on Supercomputing): Seattle WA, USA, June 2007; http://ics-conference.org
- **DATE 2007** (Design and Test in Europe): Nice, France, Apr. 2007.
- **IPDPS 2007** (21st IEEE Int. Parallel and Distributed Processing Symposium): Long Beach, CA, USA, 26-30 March 2007; http://www.ipdps.org
- **HiPEAC 2007** (Int. Conf. on High-Performance Embedded Architectures and Compilers): Ghent, Belgium, Jan. 2007; http://www.hipeac.net/hipeac2007
- **DSD'2007** (Euromicro Conf. on Digital System Design).
- **ANCS 2006** (2nd ACM/IEEE Symp. on Architectures for Networking and Communications Systems): San Jose, CA, USA, Dec. 2006.
- **ICS'06** (20th ACM Int. Conf. on Supercomputing): Queensland, Australia, June 2006.
- **DATE 2006** (Design and Test in Europe): Munich, Germany, March 2006.
- **HiPEAC 2005** (Int. Conf. on High-Performance Embedded Architectures and Compilers): Barcelona, Spain, Nov. 2005.
- **HotI 2004** (IEEE Symposium on High Performance Interconnects): Stanford, California, Aug. 2004.
- **NP3** (Workshop on Network Processors & Applications, in conjunction with HPCA): Madrid, Spain,

Feb. 2004.
- **CAC'04** (Workshop on Communication Architecture for Clusters, in conjunction with IPDPS): Santa Fe, New Mexico, USA, Apr. 2004.
- **CAC'03** (Workshop on Communication Architecture for Clusters, in conjunction with IPDPS): Nice, France, Apr. 2003.
- **ISHPC-V** (5th Intl. Symp. on High-Performance Computing): Tokyo, Japan, Oct. 2003.
- **ICS'01** (ACM Int. Conf. Supercomputing): Sorrento, Italy June, 2001.
- **ICS'00** (ACM Int. Conf. Supercomputing): Santa Fe, NM May 2000.
- **EURO-PAR 2000:** Global Chairman for "Routing and Communication in Interconnection Networks", Munich, Germany, Sep. 2000.
- **HPCS'97** (4th IEEE Workshop on the Architecture and Implementation of High Performance Communication Subsystems): Chalkidiki, Greece, June 1997.
- **EURO-PAR'95:** Stockholm, Sweden, August 1995.
- **ISCA-22** (ACM/IEEE Int. Symp. on Computer Architecture): Portofino, Italy, June 1995.
- **ISCA-20** (ACM/IEEE Int. Symp. on Computer Architecture): San Diego, CA, USA, May 1993.
- **ASPLOS IV** (ACM/IEEE Int. Conf. on Architectural Support for Programming Languages and Operating Systems): Santa Clara, CA, USA, April 1991.
- **ASPLOS III** (ACM/IEEE Int. Conf. on Architectural Support for Programming Languages and Operating Systems): Boston, MA, USA, April 1989.

4.5 Workshop Organization and Steering Committee Member:

- Katevenis was the **Main Organizer** of the Workshop *ExascaleHPC: the ExaNoDe, ExaNeSt, EcoScale, and EuroEXA projects*, held in conjunction with the HiPEAC 2018 Conference, Manchester, UK, 23 Jan. 2018; www.hipeac.net/2018/manchester/#/schedule/sessions/7521/
- Katevenis was a member of the **Steering Committee** of the 1st *AISTECS Workshop*, **2016**, on Advanced Interconnect Solutions and Technologies for Emerging Computing Systems, held in conjunction with the corresponding HiPEAC Conference; mpsoc.unife.it/~aistecs/
- Katevenis was a member of the **Steering Committee** of the 3rd through 9th *INA-OCMC Workshop*, years **2009 through 2015**, held in conjunction with the corresponding HiPEAC Conferences; mpsoc.unife.it/~inaocmc/
- Katevenis was a member of the **Steering Committee** of the *International Conference on High Performance and Embedded Architectures and Compilers (HiPEAC)*, for the years **2009 through 2012**, http://www.hipeac.net/conferences
- Katevenis was a member of the Program Committee (**PC**) of the *2nd INA-OCMC Workshop*, Goteborg, Sweden, 27 Jan. **2008**, held in conjunction with the HiPEAC 2008 Conference.
- Manolis Katevenis **organized** the *1st HiPEAC Workshop on Interconnection Network Architectures: On-Chip, Multi-Chip (INA-OCMC 2007)*, Ghent, Belgium, 28 Jan. **2007**, held in conjunction with the HiPEAC 2007 Int. Conf. on High Performance Embedded Architectures and Compilers; http://www.hipeac.net/node/716

5. Invited Lectures and Conference Presentations

last updated: July 2021

5.1 Invited Plenary Talks:

- CRISS 2019: "Modern Societal Needs: Information, Algorithmic, and Computational Thinking and Training, in Large Numbers" (Invited Keynote Speaker), *Symposium of the CRISS H2020 Project: Acquiring Digital Competence in European Education*, Heraklion, Crete, Greece, 14 November 2019; youtu.be/bpHeGMsoHdA
- FOSSCOMM 2018: "Simple and Fast Architectures, the Open RISC-V, and Low Energy Consumption" (*Keynote* Talk), *11th Panhellenic Free / Open Source Software Communities Meeting*, Heraklion, Crete, Greece, 14 October 2018; video: m.youtube.com/watch?v=qrct6XXVBBs

- PER-18: "I/O, today, is Remote (block) Load/Store, and must not be slower than Compute, any more" (Invited Presentation), *PERspectives on the Future of Computing* Workshop, held in conjunction with the HiPEAC Computing Systems Week (CSW), Goteborg (Gothenburg), Sweden, 23 May 2018; Slides: www.exanest.eu/pub/katevenis_per18_IOtoBeFast.pdf ; Video: youtube.com/watch?v=LSB3aQQ5His
- SAMOS 2017: "Cluster Communication Latency: towards approaching its Minimum Hardware Limits, on Low-Power Platforms" (Invited Presentation), *Stamatis Vassiliadis 2017 Symposium*, held in conjunction with the IEEE SAMOS XVII Conference, Samos Island, Greece, 19 July 2017; www.exanest.eu/pub/katevenis_samos17_stamatisVsymp.pdf
- AISTECS 2016: "Challenges and Opportunities in Exascale-Computing Interconnects" (*Keynote* Presentation, with N. Chrysos), *1st Int. Workshop on Advanced Interconnect Solutions and Technologies for Emerging Computing Systems (AISTECS 2016)*, held in conjunction with the HiPEAC 2016 Conference, Prague, Czech Republic, 18 Jan. 2016.
- ARTIST 2012: "Task Parallelism, Explicit Communication, and Architectural Support for them" (Invited Lecture), *Nano-Tera/Artist Summer School on Embedded System Design*, Aix-les-Bains, France, 17-21 Sep. 2012; [Abstract] - [Slides in PDF] - [Video Recording].
- "Informatics High Technology as a Tool in Medicine" (*Keynote* Talk), *Medical School Graduation Ceremony*, University of Crete, Heraklion, Greece, 15 July 2011.
- BMW 2010: "Replicate and Migrate Objects in the Runtime, not Cache Lines or Pages in Hardware" (Invited Plenary Lecture), *Barcelona Multicore Workshop 2010*, Barcelona, Spain, 21-22 Oct. 2010; [Slides in PDF].
- SAMOS 2010: "Critical Problems and Opportunities in the emerging Multi-Core Era" (Plenary Panel Member), *IEEE Int. Conf. on Embedded Computer Systems: Architectures, Modeling and Simulation*: Samos, Greece, 19-21 July 2010.
- SAMOS 2008: "Towards Unified Mechanisms for Inter-Processor Communication" (*Keynote* Presentation), *IEEE Int. Conf. on Embedded Computer Systems: Architectures, Modeling and Simulation*: Samos, Greece, 21-24 July 2008; [Slides in PDF].
- Stamatis 2007: "Interprocessor Communication seen as Load-Store Instruction Generalization" (Invited Plenary Lecture), *Stamatis Vassiliadis Symposium - The Future of Computing*, Delft, The Netherlands, 28 Sep. 2007; [Paper in PDF]. [Slides in PDF].
- OCIN 2006: "Towards Light-Weight Intra-CMP Network Interfaces" (Invited Plenary Lecture), *Workshop on On- and Off-Chip Interconnection Networks for Multicore Systems*, Stanford, California, USA, 6-7 Dec. 2006.
- **ERCIM (1993)**: "Parallel Computer Architecture: Shared Memory versus Message Passing" (Invited Lecture), Symposium of the European Research Consortium for Informatics and Mathematics (ERCIM), Rutherford Appleton Laboratory, UK, 10-12 November 1993.

5.2 Invited Lectures and Seminars:

- **U. C. Berkeley (2015)**: "Interprocessor Communication and its Interface to the Memory Hierarchy" (Invited Lecture), Computer Science Division, EECS, Univ. of California, Berkeley, CA USA, 13 February 2015.
- **U. Cyprus (2009)**: "Towards Unified Mechanisms for Inter-Processor Communication" (Invited Lecture), Computer Science Dept., University of Cyprus, Nicosia, Cyprus, 30 January 2009.
- ACACES 2007: "Queue and Flow Control Architectures for Interconnection Switches" (4-Lecture Invited Course), *3rd Int. Summer School on Advanced Computer Architecture and Compilation for Embedded Systems*, L'Aquila, Italy, 15-20 July 2007.
- **Stanford (2006)**: "Intra-CMP Light-Weight Network Interfaces, and their FPGA Prototyping" (Seminar Talk), Electrical Eng. Dept., Stanford University, California, USA, 4 December 2006.
- **T.U. Delft (2005)**: "Packet Switch Architecture and Buffered Crossbar Switches" (Seminar Talk), Electrical Eng. Dept., Delft University of Technology, The Netherlands, 10 May 2005.
- **U. of Athens (2004)**: "Digital Systems Architecture - the global situation and the position of Europe and Greece" (Invited Lecture), Dept. of Informatics, University of Athens, Greece, 1 October 2004.
- **Zappeion (2000)**: "Microelectronics and High-Speed Networks" (invited presentation to the wide public), Zappeion Exhibition and Congress Hall, Athens, Greece, May 2000.

- **Siemens (1990)**: "Forthcoming Opportunities for VLSI Electronic System Design in the Science and technology Park of Crete" (Seminar Talk), Siemens, Germany, September 1990.
- **CERN (1989)**: "The Design of the RISC II Processor at U.C.Berkeley" (Seminar Talk), CERN, Geneva, Switzerland, 25 January 1989.
- **EPY (1988)**: "Modern VLSI Technology and RISC Architectures" (Seminar Talk), Informatics Professionals Union of Greece (EPY), Athens, Greece, November 1988.
- **Stanford (1987)**: "Fast Switching and Fair Control of Congested Flow in Broad-Band Networks", Computer Systems Colloquium, Stanford University, California, USA, 2 December 1987.
- **NTUA (1987)**: "Fast Switching and Fair Control of Congested Flow in Broad-Band Networks" (Seminar Talk), National Technical University of Athens (NTUA), Greece, June 1987.
- **Air Force (1986)**: "Switching Circuit Design for Wafer-Scale Integration" (Invited Lecture), Greek Air Force Research Center, Athens, Greece, November 1986.
- **CERN (1986)**: "Design of VLSI Circuits" and "Capabilities and Limitations of VLSI Circuits" (2-lecture course), and "Reduced Instruction Set Computer Architectures" (Invited Lecture), 1986 CERN School of Computing, Geneva, Switzerland, September 1986.
- **Darmstadt (1986)**: "Reduced Instruction Set Computer Architectures for VLSI", and "Switch Design for Soft-Configurable WSI Systems" (Invited Lectures), EIS-CAD-VLSI Summer School, Technische Hochschule Darmstadt, West Germany, June 1986.
- **CAVE (1986)**: "Experience with the CAD Tools while designing the RISC II Processor" (Invited Plenary Lecture), *CAD for VLSI in Europe Workshop (CAVE)*, Patras, Greece, May 1986.
- **FACE (1985)**: "RISC Architectures" and "Soft-Configurable Wafer-Scale Integration" (Invited Lectures), FACE Research Centre, Pomezia, Italy, May 1985.
- **MIT (1984)**: "Switch Design for Soft-Configurable Wafer-Scale Integrated Systems" (Invited Lecture), Lincoln Lab, Massachusetts Institute of Technology, MA USA, 18 December 1984.
- **UMASS (1984)**: "Fast-Operand-Access- and Reduced-Instruction-Set- Computer Architectures" (Seminar Talk), University of Massachusetts at Amherst, MA USA, December 1984.
- **Stanford CIS (1984)**: "RISCy Microcomputers and Risky Wafers" (Invited Lecture), Center for Integrated Systems, Stanford University, November 1984.
- **Stanford Forum (1984)**: "Balancing Complexity and Simplicity in VLSI Design" (Invited Lecture), Computer Forum, Stanford University, February 1984.
- **Stanford CSL (1984)**: "Reduced Instructions and Fast Operand Access for General Purpose Microprocessors" (Seminar Talk), Computer Systems Lab, Stanford University, February 1984.
- **Intel (1983)**: "Designing RISC II" (Invited Lecture), Intel, Santa Clara, California, USA, 19 December 1983.
- **RISC (1983)**: "RISC Architectures for VLSI", Interview Talk, given in March 1983 at: *(i)* Bell Laboratories, Murray Hill, NJ; *(ii)* IBM, T.J.Watson Research Center; *(iii)* Carnegie-Mellon University, Pittsburgh, PA; *(iv)* Columbia University, New York, NY; *(v)* Duke University, Durham, NC; *(vi)* University of Illinois, Urbana, IL; *(vii)* Massachusetts Institute of Technology, Cambridge, MA; *(viii)* University of Maryland, College Park, MD; *(ix)* New York University, New York, NY; *(x)* Princeton University, Princeton, NJ; *(xi)* University of California, Los Angeles, CA; *(xii)* University of North Carolina, Chapel Hill, NC; *(xiii)* University of Washington, Seattle, WA; and *(xiv)* University of Wisconsin, Madison, WI.
- **Stanford CSL (1982)**: "The RISC Architecture" (Seminar Talk), Computer Systems Lab, Stanford University, November 1982.

5.3 Presentations at Conferences and Workshops:

- **EuroHPC 2019**: "ExaNeSt: Low-Latency Communication and Acceleration in a liquid-cooled energy-efficient Prototype Rack", at the *EuroHPC Summit Week - Exascale HPDA Workshop*, European Union, Poznan, Poland, 16 May 2019.
- **FET-HPC 2015**: "ExaNeSt: European Exascale System Interconnect and Storage", at the *FET-HPC Projects Workshop*, European Union, Rome, Italy, 30 Sep. 2015.
- **SAMOS 2009**: "FPGA Implementation of a Configurable Cache/Scratchpad Memory with Virtualized User-Level RDMA Capability", at the *IEEE Int. Conf. on Embedded Computer Systems: Architectures, Modeling and Simulation (IC-SAMOS IX)*: Samos, Greece, 20-23 July 2009.

- **HiPEAC IW (2008)**: "A run-time Configurable Cache/Scratchpad Memory with Virtualized User-Level RDMA Capability", at the *6th HiPEAC Industrial Workshop*, Thales Research and Technology, Palaiseau, France, 26 Nov. 2008.
- **HiPEAC IW (2006)**: "An FPGA-based Prototyping Platform for Research in High-Speed Interprocessor Communication", at the *2nd HiPEAC Industrial Workshop on Embedded Computing*, NXP Research, Eindhoven, Netherlands, 17 Oct. 2006.
- **Infocom (2006)**: "Scheduling in Non-Blocking Buffered Three-Stage Switching Fabrics", at the *IEEE Infocom 2006 Conference*, Barcelona, Spain, 23-29 Apr. 2006.
- **ICC (2004)**: "Variable Packet Size Buffered Crossbar (CICQ) Switches", at the *IEEE Int. Conf. on Communications (ICC 2004)*, Paris, France, June 2004.
- **HPSR (2003b)**: "Weighted Fairness in Buffered Crossbar Scheduling", at the *IEEE Workshop on High Performance Switching and Routing (HPSR 2003)*, Torino, Italy, June 2003.
- **HPSR (2003a)**: "Benes Switching Fabrics with O(N)-Complexity Internal Backpressure", at the *IEEE Workshop on High Performance Switching and Routing (HPSR 2003)*, Torino, Italy, June 2003.
- **ICC (2001b)**: "Efficient Per-Flow Queueing in DRAM at OC-192 Line Rate using Out-of-Order Execution Techniques", at the *IEEE Int. Conf. on Communications (ICC 2001)*, Helsinki, Finland, June 2001.
- **ICC (2001a)**: "Pipelined Heap (Priority Queue) Management for Advanced Scheduling in High Speed Networks", at the *IEEE Int. Conf. on Communications (ICC 2001)*, Helsinki, Finland, June 2001.
- **HotI (1998)**: "Implementation of ATLAS I: a Single-Chip ATM Switch with Backpressure", at the *IEEE Hot Interconnects 6 Symposium*, Stanford, California, USA, 13-15 August 1998.
- **HPCA (1998)**: "Credit-Flow-Controlled ATM for MP Interconnection: the ATLAS I Single-Chip ATM Switch" at the *4th IEEE Int. Symposium on High-Performance Computer Architecture*, Las Vegas, Nevada, Feb. 1998.
- **CANPC (1998)**: "The Remote Enqueue Operation on Networks of Workstations", at the *Workshop on Communication and Architectural Support for Network-Based Parallel Computing (CANPC)*, Las Vegas, Nevada, 31 Jan. 1998.
- **GLOBECOM (1997)**: "Switching Fabrics with Internal Backpressure using the ATLAS I Single-Chip ATM Switch", at the *IEEE GLOBECOM'97 Conference*, Phoenix, AZ USA, Nov. 1997.
- **ARVLSI (1997)**: "Pipelined Multi-Queue Management in a VLSI ATM Switch Chip with Credit-Based Flow Control", at the *17th Conference on Advanced Research in VLSI (ARVLSI)*, Ann Arbor, Michigan, Sept. 1997.

- **HPCS (1997b)**: "Buffer Requirements of Credit-Based Flow Control when a Minimum Draining Rate is Guaranteed", at the *4th IEEE Workshop on Arch. & Impl. of High Perf. Commun. Subsystems (HPCS)*, Chalkidiki, Greece, June 1997.
- **HPCS (1997a)**: "ATLAS I: Building Block for ATM Networks with Credit-Based Flow Control", at the *4th IEEE Workshop on Arch. & Impl. of High Perf. Commun. Subsystems (HPCS)*, Chalkidiki, Greece, June 1997.
- **EMSYS (1996)**: "ATLAS I: A Single-Chip ATM Switch with HIC Links and Multi-Lane Back-Pressure", at the *6th Annual Conference on Embedded Microprocessor Systems (EMSYS)*, Berlin, Germany, Sep. 1996.
- **HotI (1996)**: "ATLAS I: A General-Purpose, Single-Chip ATM Switch with Credit-Based Flow Control", at the *IEEE Hot Interconnects IV Symposium*, Stanford Univ., CA, USA, Aug. 1996.
- **SCIzzL (1995)**: "An Efficient Processor-Network Interface for Local Area Multiprocessors", at the *4th Int. Workshop on SCI-based High-Performance Low-Cost Computing*, Crete Greece, 3 October 1995.
- **SIGCOMM (1995)**: "Pipelined Memory Shared Buffer for VLSI Switches", at the *ACM SIGCOMM '95 Conference*, Cambridge, MA USA, 30 August - 1 Sep. 1995.
- **HotI (1995)**: "VC-level Flow Control and Shared Buffering in the Telegraphos Switch", at the *IEEE Hot Interconnects III Symposium*, Stanford Univ., CA, USA, Aug. 1995.
- **ERCIM (1994)**: "Where should Research on Parallel Computer Architectures focus in the next few years?" (Invited Lecture), *European Research Consortium for Informatics and Mathematics (ERCIM) PPN Workshop*, Heraklion, Crete, Greece, June 1994.
- **ASPLOS (1991)**: "Reducing the Branch Penalty by Rearranging Instructions in a Double-Width Memory", at the *4th Int. Conf. on Architectural Support for Progr. Languages and Oper. Systems (ASPLOS)*, Santa Clara, California, April 1991.

- **WSI (1986)**: "Switch Design for Soft-Configurable WSI Systems", at the *Workshop on Wafer Scale Integration - IFIP WG 10.5*, Grenoble, France, March 1986.
- **ARVLSI (1985)**: "Switch Design for Soft-Configurable WSI Systems", at the *Conference on Advanced Research in VLSI (ARVLSI)*, Chapel Hill, North Carolina, May 1985.
- **VLSI (1983)**: "The RISC II Micro-Architecture", at the *Int. Conference on Very Large Scale Integration (VLSI '83)*, Trondheim, Norway, 16-19 Aug. 1983.
- **ARVLSI (1982)**: "Datapath Design for RISC", at the *Conference on Advanced Research in VLSI (ARVLSI)*, Cambridge, Massachusetts, January 1982.

6. Graduate Students and Alumni

last updated: July 2021

6.1 Current Graduate Students:

- Orestis Moussouros
- *Co-advised with N. Chrysos*: Xenophon Vourakis, Sokratis Bartzis
- *Co-advised with V. Papaefstathiou*: Sotiris Totomis, George Matzouranis

6.2 Graduated PhD Students:

- Vassilis Papaefstathiou (PhD. December 2013; Thesis: "Architectural Support for Software-Guided Energy Reduction of Manycore Communication"; first job: Chalmers University of Technology, Gothenburg, Sweden)
- Giorgos Passas (PhD. February 2012; Thesis: "VLSI Micro-Architectures for High-Radix Crossbars"; first job: Barcelona Supercomputing Center, Spain)
- **Stamatis Kavadias** (PhD. December 2010; Thesis: "Direct Communication and Sunchronization Mechanisms in Chip Multiprocessors"; first job: Univ. of Siena, Italy)
- Nikolaos Chrysos (PhD. December 2006; Thesis: "Request-Grant Scheduling for Congestion Elimination in Multistage Networks"; first job: IBM Zurich Research Lab, Switzerland)

6.3 Distinguished Alumni:

- Andreas Moshovos, Professor, University of Toronto, recipient of the 2010 ACM Maurice Wilkes award (PhD. 1998 U.Wisconsin-Madison) (MSc. 1992 U.Crete advised by M. Katevenis - thesis: "Implementing Non-Numerical Algorithms on an Access Decoupled Architecture that supports Software Pipelining")
- Christos Kozyrakis, Professor, Stanford University, recipient of the 2015 ACM Maurice Wilkes award (PhD. 2002 U.C. Berkeley) (BSc. 1996 U.Crete advised by M. Katevenis - thesis: "The Architecture, Operation, and Design of the Queue Management Block in the ATLAS I ATM Switch")
- Stefanos Sidiropoulos, Co-Founder/CEO, Nusemi Inc., now acquired by Cadence; ex- founder, CEO, and CTO, Aeluros Inc., subsequently acquired by NetLogic Microsystems, then acquired by Broadcom (PhD. 1997 Stanford Univ.) (MSc. 1991 U.Crete advised by M. Katevenis - thesis: "Weighted Round-Robin Cell Multiplexing in a General-Purpose ATM Switch Chip")
- **Nestoras Tzartzanis**, Research Scientist, Apple (PhD. 1998 USC) (MSc. 1991 U.Crete advised by M. Katevenis - thesis: "Reducing the Branch Penalty by Rearranging Instructions in a Double-Width Memory")
- Dionisios Pnevmatikatos, Professor, National Technical University of Athens (PhD. 1995 and MSc 1991 U.Wisconsin-Madison) (BSc. 1989 U.Crete, worked with M. Katevenis on a TTL prototype using a backpressured ring to replace a tristate bus)
- Ioannis Papaefstathiou, Assoc. Professor, Aristotle University of Thessaloniki (PhD. 2000 U. Cambridge, UK) (MSc 1997 Harvard U.) (BSc. 1996 U.Crete advised by M. Katevenis - thesis: "A behavioral model of the ATLAS I switch for providing inputs and for checking the outputs of the Queue Management Block")

- Aristides Efthymiou, Assistant Professor, University of Ioannina (PhD. 2002 U. Manchester) (MSc. 1995 U.Crete advised by M. Katevenis - thesis: "Design, Implementation, and Testing of a 25 Gb/s Pipelined Memory Switch Buffer in Full-Custom CMOS").
- Nikos Hardavellas, Assoc. Professor, Northwestern University, Evanston, IL USA (PhD. 2009 and MSc. 2006 CMU) (BSc. 1995 U.Crete advised by M. Katevenis).
- Georgios Michelogiannakis, Research Scientist, Lawrence Berkeley National Lab, CA USA (PhD. 2012 Stanford U.) (MSc. 2007 and BSc. 2005 U.Crete advised by M. Katevenis).

6.4 Graduated MSc Students:

- 2021: *Co-advised with V. Papaefstathiou*: **Iason Mastorakis**, **Sotirios Totomis**.
- 2020: *Co-advised with N. Chrysos*: **Evangelos Mageiropoloulos**. *Co-advised with V. Papaefstathiou*: **Michael Giaourtas**. *Co-advised with N. Kallimanis*: **Charidimos Kiosterakis**.
- 2019: *Co-advised with N. Chrysos*: **Antonis Psistakis**, **Pantelis Xirouchakis**, **Leandros Tzanakis-Arnaoutakis**. *Co-advised with M. Marazakis*: **Manolis Skordalakis**. *Co-advised with M. Marazakis and M. Ploumidis*: **Ioannis Vardas**.
- 2017: *Co-advised with N. Chrysos*: **Dimitrios Giannopoulos**.
- 2015: **Evangelos Vassilakis**. *Co-advised with M. Marazakis*: **Yiannis Velegrakis**, **Dimitrios Poulios**. *Co-advised with P. Pratikakis*: **Apostolos Glenis**.
- 2013: **Antonis Psathakis**.
- 2011: **Dimitris Tsaliagos**.
- 2009: **Georgios Nikiforos**.
- 2007: Michael Papamichael, Georgios Michelogiannakis.
- 2006: **Giorgos Passas**, Evangelos Vlachos.
- 2004: **Dimitris Simos**.
- 2002: Nikolaos Chrysos, **Giorgos Sapountzis**, **Spyros Lyberis**, **Costas Harteros**, **Dimitris Capsalis**, **Dimitris Meidanis**.
- 2001: **Christos Lolas**, **George Papadakis**.
- 2000: **Aggelos Ioannou**, **Aris Nikologiannis**.
- 1998: **Georgios Glykopoulos**.
- 1997: **Georgios Kornaros**.
- 1996: **Manolis Spyridakis**.
- 1995: Aristides Efthymiou.
- 1994: **Giorgos Dimitriadis**, **Maria Karavassili**, **Chara Xanthaki**.
- 1993: **Iasson Farsaris**, **Nikos Karydis**.
- 1992: Andreas Moshovos, **Peny Vatsolaki**, **Achileas Mantzios**, **Christos Georgis**, **Panagiotis Kalogerakis**, **Tassos Sorilos**.
- 1991: Stefanos Sidiropoulos, **Nestoras Tzartzanis**.
- 1990: **Vaggelis Halkiadakis**.

6.5 Member (other than Chair) of PhD Thesis Committees:

- **Tassos Papagiannis**, Univ. of Crete, Greece (2015-21)
- **Anastasios Psarras**, Democritos Univ. of Thrace, Greece (2017)
- **Foivos Zakkak**, Univ. of Crete, Greece (2015-16)
- **Nikos Foutris**, Univ. of Athens, Greece (2015)
- **Iakovos Mavroidis**, **Evripidis Sotiriadis**, **Kyprianos Papadimitriou**, **Antonis Nikitakis**, **Grigorios Chrysos**, Technical Univ. of Crete, Chania, Greece (2011-14)
- **Spyros Lyberis**, **Pavlos Matthaiakis**, Univ. of Crete, Greece (2013)
- **German Rodriguez**, UPC, Barcelona, Spain (2011)
- **Evriklis Kounalakis**, Univ. of Crete, Greece (2011)
- **Miquel Moreto**, UPC, Barcelona, Spain (2010)
- **Lotfi Mhamdi**, T.U. Delft, Netherlands (2007)
- **Pedro Javier Garcia**, UCLM, Spain (2006)

7. Courses taught, New Courses introduced

last updated: July 2021

7.1 Courses Taught:

- CS-534 - Packet Switch Architecture: Graduate course, CS Dept., Univ. of Crete (taught 14 times: Sp'96, Sp'98, and Sp'00 with Stamoulis; F'01, Sp'03, Sp'04, Sp'05, Sp'06, Sp'07, Sp'08, Sp'09, Sp'11, Sp'13; Sp'15 with N. Chrysos; taught by Nikolaos Chrysos alone after 2015).
- CS-120 - Digital Design: first-year undergraduate core course, CS Dept., Univ. of Crete (taught 21 times: F'85, F'02, F'03, F'04, F'05, F'06, F'07, F'08, F'09, F'10, F'11, F'12, F'13, F'14, F'15, F'16, F'17, F'18, F'19, F'20, F'21).
- CS-121 - Electric Circuits: Undergraduate introductory elective course, CS Dept., Univ. of Crete (taught 3 times: Sp'10, Sp'11, Sp'12).
- CS-225 - Computer Organization: second-year undergraduate core course, CS Dept., Univ. of Crete (taught 24 times: Sp'86, Sp'87, F'93, Sp'96; Sp'99 with Serpanos; Sp'01, Sp'02; Sp'03 with I. Papaefstathiou; Sp'04 through Sp'08 with Bilas; Sp'09 with Nikolopoulos; Sp'12 and Sp'13 with Sotiriou; Sp'14, Sp'15, Sp'16, Sp'17, Sp'18, Sp'19, Sp'20, Sp'21).
- **CS-425 - Computer Architecture**: Senior undergraduate / introductory graduate elective course, CS Dept., Univ. of Crete (taught 13 times: Sp'86, F'88, F'89, Sp'91, F'92, Sp'94, F'96, F'99, F'00, F'03 with Bilas and Y. Papaefstathiou, F'04 with Bilas and J. Mavroidis, F'05 and F'06 with Bilas and Karlsson)
- **CS-625 - Advanced Computer Architecture**: Graduate course, CS Dept., Univ. of Crete (taught 3 times: Sp'90, Sp'92, Sp'01)
- **CS-422 - Introduction to VLSI Systems**: Senior undergraduate / introductory graduate elective course, CS Dept., Univ. of Crete (taught 9 times: Sp'87, Sp'89, Sp'91, Sp'93, Sp'95, Sp'98, F'99, F'00, F'02 with Sotiriou)
- **CS-523 - Computer Aided Design of Digital Systems**: Graduate course, CS Dept., Univ. of Crete (taught twice: F'85, Sp'01)
- **CS-520 - Semi-Custom ASIC Design**: Graduate course, CS Dept., Univ. of Crete (taught with Papadourakis in Sp'92)
- **CS-321 - Digital MOS Electronic Circuits**: Undergraduate elective course, CS Dept., Univ. of Crete (taught 5 times, with Traganitis: F'88, F'89, F'90, F'92, F'94)
- **CS-320 - Microprocessors and Peripherals**: Undergraduate elective course, CS Dept., Univ. of Crete (taught F'86)
- **CS-345 - Operating Systems**: Undergraduate core course, CS Dept., Univ. of Crete (taught twice: Sp'88, Sp'89)
- **CS-240 - Data Structures**: Undergraduate core course, CS Dept., Univ. of Crete (taught F'90)
- **CS-100 - Introduction to Computer Science**: Undergraduate core course, CS Dept., Univ. of Crete (taught twice: F'95, F'98)

- **EE-271 - Introduction to VLSI Systems**: Senior undergraduate / introductory graduate course, Electrical Eng. Dept., *Stanford University* (taught twice: Winter'85, F'87)
- **EE-272A - Design Projects in VLSI Systems**: Senior undergraduate / introductory graduate course, Electrical Eng. Dept., *Stanford University* (taught Winter'84)
- **CS-311 - Computer Systems Architecture**: Graduate course, Computer Sci. Dept., *Stanford University* (taught twice: Sp'84; F'84 with F. Baskett)

- ACACES 2007: "Queue and Flow Control Architectures for Interconnection Switches" (4-Lecture Invited Course), *3rd Int. Summer School on Advanced Computer Architecture and Compilation for Embedded Systems*, L'Aquila, Italy, 15-20 July 2007.

7.2 New Courses Introduced:

- Within the European Research Center on Computer Architecture (EuReCCA), Katevenis proposed and coordinated the initial setup of *Joint Graduate Courses via video-conferencing*, starting in Spring 2012 with the courses: Applied CUDA Programming and CMOS Technology for Computer Architects
- CS-534 - Packet Switch Architecture (graduate course, CS Dept., Univ. of Crete): course content has been innovative world-wide to some extent, partly based on own research results.
- CS-120 - Digital Design (1st year undergraduate core course, CS Dept., Univ. of Crete): course content developed for the specific teaching requirements, including our custom Lab Equipment (photo) and a novel datapath board of ours for a very simple computer (photo).
- CS-225 - Computer Organization (2nd year undergraduate core course, CS Dept., Univ. of Crete): course content developed for the specific teaching requirements, including the specific set of exercises and simulation mini-project.
- CS-121 - Electric Circuits (1st year undergraduate elective course, CS Dept., Univ. of Crete): developed an extensive set of Laboratory exercises.
- At the University of Crete, CS Dept., Katevenis was the first to teach the following courses, having thus contributed to adapting their content to the specific environment: **CS-425**, **CS-625**, **CS-422**, **CS-423**, **CS-321**, **CS-320**,
- At Stanford University, in 1984-85, Katevenis reorganized the laboratory and the exercises of the **EE-271/272A (VLSI Design)** courses, using –for the first time– colour workstations and graphics editors.

7.3 Wider-Community Education and Training Activities – Distinctions:

- **Video-recorded Open Courses**: the Fall 2013 offering of the Digital Design (CS-120) course and the Spring 2014 offering of the Computer Organization (CS-225) course were video-recorded and are since then available to the general public through opencourses.uoc.gr (CS-120 - CS-225) – also on Youtube: goo.gl/jY4qVk with **41 thousand views**. Similar recordings in 2020-2021, during the covid-19 pandemic, when these courses were offered via teleconference.
- **Open Courses Distinction Award**: in October 2015, the OpenCourses.gr organization awarded distinctions to the best one percent (1%) among their almost 3000 open courses. Digital Design (CS-120) by Manolis Katevenis won one of these Distinction Awards.
- During HiPEAC-2 (**2008-2012**), Katevenis led the Task Force on Education and Training of HiPEAC –the European Network of Excellence in High-Performance and Embedded Architecture and Compilation.
- Katevenis was the lead-organizer of the *Tutorial: "Teaching Introductory Computer Architecture and Programming: What, When, How?"* held in conjunction with: the 5th Int. Conference on High-Performance and Embedded Architectures and Compilers (HiPEAC) 2010, 24 January **2010**, Pisa, Italy.
- Local Organizer, NetFPGA Hands-On Tutorial, FORTH, Crete, Greece, 16-17 September **2010**.

- M. Katevenis: "From Multiplexors and Trees to Memories and Processors: The Digital Design Lab of the University of Crete meets the High-School Students of Crete", Lecture (and Lab Equipment Demo by G. Kalokerinos) during the *4th Heraklion Digital Creation High-School Student Festival* (Digifest), Heraklion City Center (Androgeo Hall), Crete, Greece, 5 April **2014**.
- M. Katevenis: "Recent Trends in Computer Architecture and Teaching Methodologies in Digital Systems", 3-hour *Training Tutorial for High-School Informatics Teachers of East Crete*, FORTH, Crete, Greece, 8 February **2012**.
- M. Katevenis: "The Hardware infrastructure for Informatics: from Digital Circuits to Computer Architecture", 3-hour Seminar during the 3-day Summer *Training Course for High-School Informatics Teachers of Greece*, Centre for Education and Sciences, Patras, Greece, 7-9 July **2010**.